[1] The amendment filed on 4/30/10 is entered and made of record.

[2] EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with David Hall on 5/26/10.

The application has been amended as follows:

I. With regards to claim 1, replace the following:

"1. A defect data analysis method comprising the steps of:

obtaining defect position information by inspecting a substrate with an inspection apparatus, wherein the substrate is processed in a process of circuit pattern formation on the substrate;

storing the obtained defect position information in memory;

processing the defect position information stored in the memory using a processor;

obtaining a defect distribution pattern on a wafer map from the processed defect position information, the defect distribution pattern representing a placement state of a plurality of defects on the wafer map;

classifying the obtained defect distribution pattern on the wafer map into one of a plurality of distribution regional defect categories by using a defect distribution shape pattern classifier and the processed defect position information, wherein the plurality of regional defect categories comprises: repeated defects, clustered defects, arc-shaped regional defects, radial regional defects, line type regional defects, ring and blob type regional defects and random defects; and displaying, on a display screen, the classified defect distribution pattern relative to the wafer map, wherein the characteristic regional defect categories are each displayed using different colors." **with**

--1. A defect data analysis method comprising the steps of:

obtaining defect position information by inspecting a substrate with an inspection apparatus, wherein the substrate is processed in a process of circuit pattern formation on the substrate;

storing the obtained defect position information in memory;

processing the defect position information stored in the memory using a processor;

obtaining a defect distribution pattern on a wafer map from the processed defect position information, the defect distribution pattern representing a placement state of a plurality of defects on the wafer map;

classifying the obtained defect distribution pattern on the wafer map into one of a plurality of distribution regional defect categories by using a defect distribution shape pattern classifier and the processed defect position information, wherein the plurality of regional defect categories comprises: repeated defects, clustered defects, arc-shaped regional defects, radial

regional defects, line type regional defects, ring and blob type regional defects and random defects; and

displaying, on a display screen, the classified defect distribution pattern relative to the wafer map, wherein the characteristic regional defect categories are each displayed using different colors,

wherein the radial regional defects are detected by creating distribution data on a $\rho\ \theta$ space based on information associated with the defects distributed on the processed substrate on Cartesian coordinate space and extracting the radial regional defects from the distribution data on the $\rho\ \theta$ space, further comprising:

converting the information associated with the defects distributed on the processed substrate on the Cartesian coordinate space into the defect position information on the polar coordinate space by using:

a distance between a straight line connecting two arbitrary defects on the processed substrate and an origin of the Cartesian coordinate space, and

an angle defined by an X axis and a perpendicular drawn from the origin of the Cartesian coordinate space to a straight line connecting two arbitrary defects.--

II. With regards to claim 7, replace the following:

"7. A defect data analysis method comprising the steps of:

obtaining defect distribution information on a processed substrate from defect position information, obtained by inspecting the processed substrate with an inspection apparatus, the substrate being processed in a process for forming a circuit pattern on the substrate;

storing the obtained defect distribution information in memory;

processing the stored defect distribution information using a processor to obtain a defect distribution pattern representing a placement state of a plurality of defects on a wafer map;

identifying a repeated defect in the defect distribution pattern by using the wafer map, wherein the repeated defect comprises defects which are distributed on the substrate in a repeated pattern;

identifying a clustered defect in the defect distribution pattern by using the wafer map, wherein the clustered defect comprises defects which are distributed on the substrate in a cluster;

identifying an arc-shaped regional defect in the defect distribution pattern by using the wafer map, wherein the arc-shaped regional defect comprises defects which are distributed on the substrate in an arc-shape;

identifying a radial regional defect in the defect distribution pattern by using the wafer map, wherein the radial regional defect comprises defects which are radially distributed on the substrate;

identifying a line type regional defect in the defect distribution pattern by using the wafer map, wherein the line type regional defect comprises defects which are linearly distributed on the substrate;

identifying ring and blob type regional defect in the defect distribution pattern by using the wafer map, wherein the ring and blob type regional defects comprise defects which are distributed on the substrate in a ring and blob shape;

identifying a random defect in the defect distribution pattern by using the wafer map, wherein the random defect comprises defects which are randomly distributed on the substrate;

classifying the identified defects using the processor into corresponding regional defect categories; and

displaying the processed information on the wafer map displayed on a display screen, wherein the processed information is displayed such that the different regional defect categories are displayed using different colors." **with**

--7. A defect data analysis method comprising the steps of:

obtaining defect distribution information on a processed substrate from defect position information, obtained by inspecting the processed substrate with an inspection apparatus, the substrate being processed in a process for forming a circuit pattern on the substrate;

storing the obtained defect distribution information in memory;

processing the stored defect distribution information using a processor to obtain a defect distribution pattern representing a placement state of a plurality of defects on a wafer map;

identifying a repeated defect in the defect distribution pattern by using the wafer map, wherein the repeated defect comprises defects which are distributed on the substrate in a repeated pattern;

identifying a clustered defect in the defect distribution pattern by using the wafer map, wherein the clustered defect comprises defects which are distributed on the substrate in a cluster;

identifying an arc-shaped regional defect in the defect distribution pattern by using the wafer map, wherein the arc-shaped regional defect comprises defects which are distributed on the substrate in an arc-shape;

identifying a radial regional defect in the defect distribution pattern by using the wafer map, wherein the radial regional defect comprises defects which are radially distributed on the substrate;

identifying a line type regional defect in the defect distribution pattern by using the wafer map, wherein the line type regional defect comprises defects which are linearly distributed on the substrate;

identifying ring and blob type regional defect in the defect distribution pattern by using the wafer map, wherein the ring and blob type regional defects comprise defects which are distributed on the substrate in a ring and blob shape;

identifying a random defect in the defect distribution pattern by using the wafer map, wherein the random defect comprises defects which are randomly distributed on the substrate;

classifying the identified defects using the processor into corresponding regional defect categories; and

displaying the processed information on the wafer map displayed on a display screen, wherein the processed information is displayed such that the different regional defect categories are displayed using different colors,

wherein the radial regional defects are detected by creating distribution data on a $\rho\ \theta$ space based on information associated with the defects distributed on the processed substrate on Cartesian coordinate space and extracting the radial regional defects from the distribution data on the $\rho\ \theta$ space, further comprising:

converting the information associated with the defects distributed on the processed substrate on the Cartesian coordinate space into the defect position information on the polar coordinate space by using:

a distance between a straight line connecting two arbitrary defects on the processed substrate and an origin of the Cartesian coordinate space, and

an angle defined by an X axis and a perpendicular drawn from the origin of the Cartesian coordinate space to a straight line connecting two arbitrary defects.--

III. With regards to claim 12, replace the following:

"12. A defect data analysis apparatus comprising:

input means for inputting defect position information obtained by inspecting a processed substrate, wherein the substrate is processed by forming a circuit pattern on the substrate;

defect distribution calculation means for obtaining a defect distribution pattern on a wafer map from the defect position information, the defect distribution pattern representing a placement state of a plurality of defects on a wafer map;

regional defect distribution shape classification means for classifying the defect distribution pattern to one of a plurality of regional defect categories comprising: repeated defects, clustered defects, arc-shaped regional defects, radial regional defects, line type regional defects, ring and blob type regional defects, and random defects, wherein the classifying is performed based on the defect position information; and

output means for outputting the classified defect distribution pattern relative to the wafer map."

with

--12. A defect data analysis apparatus comprising:

input means for inputting defect position information obtained by inspecting a processed substrate, wherein the substrate is processed by forming a circuit pattern on the substrate;

defect distribution calculation means for obtaining a defect distribution pattern on a wafer map from the defect position information, the defect distribution pattern representing a placement state of a plurality of defects on a wafer map;

regional defect distribution shape classification means for classifying the defect distribution pattern to one of a plurality of regional defect categories comprising: repeated defects, clustered defects, arc-shaped regional defects, radial regional defects, line type regional defects, ring and blob type regional defects, and random defects, wherein the classifying is performed based on the defect position information; and

output means for outputting the classified defect distribution pattern relative to the wafer map,

wherein the radial regional defects are detected by creating distribution data on a $\rho\ \theta$ space based on information associated with the defects distributed on the processed substrate on Cartesian coordinate space and extracting the radial regional defects from the distribution data on the $\rho\ \theta$ space, further comprising:

converting the information associated with the defects distributed on the processed substrate on the Cartesian coordinate space into the defect position information on the polar coordinate space by using:

a distance between a straight line connecting two arbitrary defects on the processed substrate and an origin of the Cartesian coordinate space, and

an angle defined by an X axis and a perpendicular drawn from the origin of the Cartesian coordinate space to a straight line connecting two arbitrary defects.--

IV. With regards to claim 14, replace the following:

"14. A review system comprising:

an inspection apparatus for scanning a surface of a processed substrate by light or electronic beam to detect a foreign matter or a pattern defect on the processed substrate and outputting defect data comprising at least position coordinates of the detected foreign matter or the pattern defect; and

a defect data analysis apparatus for obtaining a defect distribution pattern on a wafer map using the position coordinates, the defect distribution pattern representing a placement state of a plurality of defects on the wafer and for classifying the defect distribution pattern into one of a plurality of regional defect categories, wherein the plurality of regional defect categories comprises: repeated defects, clustered defects, arc shaped regional defects, radial regional defects, line type regional defects, ring and blob type regional defects, and random defects, wherein an image of the defect distribution pattern is acquired by the light or the electron beam."

with

--14. A review system comprising:

an inspection apparatus for scanning a surface of a processed substrate by light or electronic beam to detect a foreign matter or a pattern defect on the processed substrate and outputting defect data comprising at least position coordinates of the detected foreign matter or the pattern defect; and

a defect data analysis apparatus for obtaining a defect distribution pattern on a wafer map using the position coordinates, the defect distribution pattern representing a placement state of a plurality of defects on the wafer and for classifying the defect distribution pattern into one of a plurality of regional defect categories, wherein the plurality of regional defect categories comprises: repeated defects, clustered defects, arc shaped regional defects, radial regional defects, line type regional defects, ring and blob type regional defects, and random defects, wherein an image of the defect distribution pattern is acquired by the light or the electron beam,

wherein the radial regional defects are detected by creating distribution data on a $\rho\ \theta$ space based on information associated with the defects distributed on the processed substrate on Cartesian coordinate space and extracting the radial regional defects from the distribution data on the $\rho\ \theta$ space, further comprising:

converting the information associated with the defects distributed on the processed substrate on the Cartesian coordinate space into the defect position information on the polar coordinate space by using:

a distance between a straight line connecting two arbitrary defects on the processed substrate and an origin of the Cartesian coordinate space, and

an angle defined by an X axis and a perpendicular drawn from the origin of the Cartesian coordinate space to a straight line connecting two arbitrary defects.--

[3] REASONS FOR ALLOWANCE

Claims 1-7 and 9-17 are allowable.

With regards to claim 1, the examiner cannot find any applicable prior art providing teachings for the following limitations:

wherein the radial regional defects are detected by creating distribution data on a $\rho\ \theta$ space based on information associated with the defects distributed on the processed substrate on Cartesian coordinate space and extracting the radial regional defects from the distribution data on the $\rho\ \theta$ space, further comprising:

converting the information associated with the defects distributed on the processed substrate on the Cartesian coordinate space into the defect position information on the polar coordinate space by using:

a distance between a straight line connecting two arbitrary defects on the processed substrate and an origin of the Cartesian coordinate space, and
an angle defined by an X axis and a perpendicular drawn from the origin of the Cartesian coordinate space to a straight line connecting two arbitrary defects in combination with the rest of the limitations of claim 1.

With regards to claims 7, 12 and 14, see the rationale for claim 1.

With regards to claim 10, the examiner cannot find applicable prior art and / or suggestion disclosing weighting a point where a perpendicular of arbitrary two defects from the wafer map passes according to the distance between the two defects and voting the point onto the xy space and detecting (x,y) corresponding to the maximum value on the voted space in combination with the rest of the limitations of claim 10.

With regards to claim 11, see the rationale and rejection for claim 10.

[4] RELEVANT ART

I. Tsutsui (US pat no 6,009,545): Tsutsui discloses

obtaining defect position information by inspecting a substrate with an inspection apparatus, wherein the substrate is processed in a process of circuit pattern formation on the substrate (see figure 1, section 3, stores position information of defects);

storing the obtained defect position information in memory (see figure 1, the position information are stored);

processing the defect position information stored in the memory using a processor; obtaining a defect distribution pattern on a wafer map from the processed defect position information, the defect distribution pattern representing a placement state of a plurality of defects on the wafer map (see figures 10 and 13, shows defect distribution).

Tsutsui does not disclose

classifying the obtained defect distribution pattern on the wafer map into one of a plurality of distribution regional defect categories by using a defect distribution shape pattern

classifier and the processed defect position information, wherein the plurality of regional defect categories comprises: repeated defects, clustered defects, arc-shaped regional defects, radial regional defects, line type regional defects, ring and blob type regional defects and random defects; and displaying, on a display screen, the classified defect distribution pattern relative to the wafer map, wherein the characteristic regional defect categories are each displayed using different colors.

II. Kulkarni (US pat no 5,991,699): Kulkarni discloses classifying the obtained defect distribution pattern on the wafer map into one of a plurality of distribution regional defect categories by using a defect distribution shape pattern classifier and the processed defect position information (see figure 3, 114).

Kulkarni is silent in

wherein the radial regional defects are detected by creating distribution data on a $\rho\ \theta$ space based on information associated with the defects distributed on the processed substrate on Cartesian coordinate space and extracting the radial regional defects from the distribution data on the $\rho\ \theta$ space, further comprising:

converting the information associated with the defects distributed on the processed substrate on the Cartesian coordinate space into the defect position information on the polar coordinate space by using:

a distance between a straight line connecting two arbitrary defects on the processed substrate and an origin of the Cartesian coordinate space, and

an angle defined by an X axis and a perpendicular drawn from the origin of the Cartesian coordinate space to a straight line connecting two arbitrary defects.

[5] Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALEX LIEW whose telephone number is (571)272-8623 (FAX 571-273-8623) or cell (917)763-1192. The examiner can be reached anytime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on (571) 272-7332. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vu Le/
Supervisory Patent Examiner, Art Unit 2624

/Alex Liew/
AU2624
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